

Form PTO-1449		ATTORNEY DOCKET NO. AUS920040064US1	SERIAL NO. 10/806,871		
LIST OF PRIOR ART CITED BY APPLICANT <small>(Use several sheets if necessary)</small>		APPLICANT Dimpsey et al. FILING DATE March 22, 2004 GROUP ART UNIT 2185			
U.S. PATENT DOCUMENTS					
EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE
A.S.	AA 5,103,394	Apr. 7, 1992	Blasciak	395/575	Dec. 21, 1989
	AB 6,330,662 B1	Dec. 11, 2001	Patel et al.	712/236	Feb. 23, 1999
	AC 6,480,938 B2	Nov. 12, 2002	Vondran, Jr.	711/125	Dec. 15, 2000
	AD 6,430,741 B1	Aug. 6, 2002	Mattson, Jr. et al.	717/154	Feb. 26, 1999
	AE 6,189,141 B1	Feb. 13, 2001	Benitez et al.	717/4	May 4, 1998
	AF 5,930,508	Jul. 27, 1999	Faraboschi et al.	395/706	Jun. 9, 1997
	AG 6,351,844 B1	Feb. 26, 2002	Bala	717/4	Nov. 5, 1998
	AH 6,324,689 B1	Nov. 27, 2001	Lowney et al.	717/9	Sep. 30, 1998
	AI 6,442,585 B1	Aug. 27, 2002	Dean et al.	709/108	Nov. 26, 1997
	AJ 5,774,724	Jun. 30, 1998	Heisch	395/704	Nov. 20, 1995
	AK 5,987,250	Nov. 16, 1999	Subrahmanyam	395/704	Aug. 21, 1997
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	AN 6,223,338 B1	Apr. 24, 2001	Smolders	717/4	Sep. 30, 1998
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	AQ 6,446,029 B1	Sep. 3, 2002	Davidson et al.	702/186	Jun. 30, 1999
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	AS 5,937,437	Aug. 10, 1999	Roth et al.	711/202	Oct. 28, 1996
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	AV 5,938,778	Aug. 17, 1999	John, Jr. et al.	714/45	Nov. 10, 1997
	AW 6,286,132 B1	Sep. 4, 2001	Tanaka et al.	717/4	Jan. 7, 1999
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	AY 6,374,364 B1	Apr. 16, 2002	McElroy et al.	714/10	Jan. 19, 1999
✓	AZ 6,070,009	May 30, 2000	Dean et al.	395/704	Nov. 26, 1997
A.S.	BA 5,966,537	Oct. 12, 1999	Ravichandran	395/709	May 28, 1997
DATE CONSIDERED 9/18/06			EXAMINER <i>Augie Andy</i>		
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					

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			FILING DATE March 22, 2004	GROUP ART UNIT-2465-2185		
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EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE	
A.S.	BB 2002/0129309	Sep. 12, 2002	Floyd et al.	714/724	Dec. 18, 2000	
	BC 2001/0032305	Oct. 18, 2001	Barry	712/34	Feb. 23, 2001	
	BD 2002/0199179	Dec. 26, 2002	Lavery et al.	717/158	Jun. 21, 2001	
	BE 2002/0124237	Sep. 5, 2002	Sprunt et al.	717/127	Dec. 29, 2000	
✓	BF 2002/0147965	Oct. 10, 2002	Swaine et al.	717/124	Feb. 1, 2001	
A.S.	BG 2002/0019976	Feb. 14, 2002	Patel et al.	717/137	May 25, 2001	
FOREIGN PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO	
A.S.	BH JP2000029731	Dec. 8, 1999	Japan	G06F 9/38	X	
A.S.	BI JP2000347863	Dec. 15, 2000	Japan	G06F 9/38	X	
OTHER PRIOR ART (including author, title, date, pertinent page, etc.)						
BJ	Kikuchi, "Parallelization Assist System", <i>Johe Shori</i> , Vol. 34, No. 9, Sept. 1993, pp. 1158-1169.					
A.S.	BK	Cohen et al., "Hardware-Assisted Characterization of NAS Benchmarks", <i>Cluster Computing</i> , Vol. 4, No. 3, July 2001, pp. 189-196.				
	BL	Talla et al., "Evaluating Signal Processing and Multimedia Applications on SIMD, VLIW and Super Scalar Architectures", <i>International Conference on Computer Design</i> , Austin, Sept. 17-20, 2000, pp. 163-172.				
	BM	Iwasawa et al., "Parallelization Method of Fortran DO Loops by Parallelizing Assist System", <i>Transactions of Information Processing Society of Japan</i> , Vol. 36, No. 8, Aug. 1995, pp. 1995-2006.				
↓	BN	Talla et al., "Execution Characteristics of Multimedia Applications on a Pentium II Processor", <i>IEEE International Performance, Computing, and Communications Conference</i> , 19 th , Phoenix, Feb. 20-22, 2000, pp. 516-524.				
A.S.	BO	IBM Research Disclosure Bulletin 444188, "Enable Debuggers as an Objective Performance Measurement Tool for Software Development Cost Reduction", April 2001, pp. 686-688.				
RELATED PATENT APPLICATIONS						
EXAMINER INITIAL	APPLICATION NO./ ATTY. DOCKET NO.	APPLICANT	TITLE		FILING DATE	
A.S.	BP 09/435,069 AT9-99-491	Davidson et al.	Method and Apparatus for Instruction Sampling for Performance Monitoring and Debug		Nov. 4, 1999	
A.S.	BQ 08/538,071 AUT919950055US1	Gover et al.	Method and System for Selecting and Distinguishing an Event Sequence using an Effective Address in a Processing System		Oct. 2, 1995	
DATE CONSIDERED 9/18/06			EXAMINER <i>Chapman</i> <i>Asch</i>			
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LIST OF PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)			APPLICANT Dimpsey et al.	
			FILING DATE March 22, 2004	GROUP ART UNIT 2165 2185
RELATED PATENT APPLICATIONS				
EXAMINER INITIAL	APPLICATION NO./ ATTY. DOCKET NO.	APPLICANT	TITLE	
A.S.	BR 10/675,777 / AUS920030477US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Instruction Execution and Data Accesses	
	BS 10/674,604 / AUS920030478US1	DeWitt, Jr. et al.	Method and Apparatus for Selectively Counting Instructions and Data Accesses	
	BT 10/675,831 / AUS920030479US1	DeWitt, Jr. et al.	Method and Apparatus for Generating Interrupts Upon Execution of Marked Instructions and Upon Access to Marked Memory Locations	
	BU 10/675,778 / AUS920030480US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Data Accesses and Instruction Executions that Exceed a Threshold	
	BV 10/675,776 / AUS920030481US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Execution of Specific Instructions and Accesses to Specific Data Locations	
	BW 10/675,751 / AUS920030482US1	DeWitt, Jr. et al.	Method and Apparatus for Debug Support for Individual Instructions and Memory Locations	
	BX 10/675,721 / AUS920030483US1	Levine et al.	Method and Apparatus to Autonomically Select Instructions for Selective Counting	
	BY 10/674,642 / AUS920030484US1	Levine et al.	Method and Apparatus to Autonomically Count Instruction Execution for Applications	
	BZ 10/674,606 / AUS920030485US1	Levine et al.	Method and Apparatus to Autonomically Take an Execution on Specified Instructions	
	CA 10/675,783 / AUS920030486US1	Levine et al.	Method and Apparatus to Autonomically Profile Applications	
	CB 10/675,872 / AUS920030487US1	DeWitt, Jr. et al.	Method and Apparatus for Counting Instruction and Memory Location Ranges	
	CC 10/757,250 / AUS920030488US1	Levine et al.	Method and Apparatus for Maintaining Performance Monitoring Structures in a Page Table for use in Monitoring Performance of a Computer Program	
✓	CD 10/757,192 / AUS920030543US1	DeWitt, Jr. et al.	Method and Apparatus for Providing Pre and Post Handlers for Recording Events	
A.S.	CE 10/757,192 / AUS920030548US1	DeWitt, Jr. et al.	Method and Apparatus for Determining Computer Program Flows Autonomically Using Hardware Assisted Thread Stack Tracking and Cataloged Symbolic Data	
DATE CONSIDERED 9/18/06		EXAMINER <i>Linda S. Saito</i>		
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EXAMINER INITIAL	APPLICATION NO / ATTY. DOCKET NO.	APPLICANT	TITLE	FILING DATE
A.S.	CF 10/757,227 / AUS920030555US1	DeWitt, Jr. et al.	Method and Apparatus for Autonomically Moving Cache Entries to Dedicated Storage when False Cache Line Sharing is Detected	Jan. 14, 2004
	CG 10/757,197 / AUS920030556US1	DeWitt, Jr. et al.	Method and Apparatus for Optimizing Code Execution Using Annotated Trace Information having Performance Indicator and Counter Information	Jan. 14, 2004
	CH 10/807,094 / AUS920040059US1	Dimpsey et al.	Method and Apparatus for Providing Hardware Assistance for Code Coverage	Mar. 22, 2004
	CI 10/808,716 / AUS920040060US1	Dimpsey et al.	Method and Apparatus for Autonomic Test Case Feedback Using Hardware Assistance for Code Coverage	Mar. 22, 2004
	CJ 10/806,576 / AUS920040061US1	Dimpsey et al.	Method and Apparatus for Hardware Assistance for Data Access Coverage	Mar. 22, 2004
	CK 10/806,633 / AUS920040062US1	Dimpsey et al.	Method and Apparatus for Providing Hardware Assistance for Data Access Coverage on Dynamically Allocated Data	Mar. 22, 2004
✓	CL 10/806,917 / AUS920040063US1	Dimpsey et al.	Method and Apparatus for Autonomic Test Case Feedback Using Hardware Assistance for Data Coverage	Mar. 22, 2004
A.S.	CM 10/806,866 / AUS920040065US1	Dimpsey et al.	Method and Apparatus for Prefetching Data from a Data Structure	Mar. 22, 2004
DATE CONSIDERED 9/18/06		EXAMINER <i>lynch, fahy</i>		
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<table border="1"> <tr> <td>Application Number</td> <td>10/806,871</td> </tr> <tr> <td>Filing Date</td> <td>03-22-2004</td> </tr> <tr> <td>First Named Inventor</td> <td>Dimpsey et al.</td> </tr> <tr> <td>Examiner Name</td> <td>Popovici, Boz Arpsn Savik</td> </tr> <tr> <td>Art Unit</td> <td>2165 2185</td> </tr> <tr> <td>Attorney Docket No.</td> <td>AUS920040064US1</td> </tr> </table>			Application Number	10/806,871	Filing Date	03-22-2004	First Named Inventor	Dimpsey et al.	Examiner Name	Popovici, Boz Arpsn Savik	Art Unit	2165 2185	Attorney Docket No.	AUS920040064US1
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Examiner Name	Popovici, Boz Arpsn Savik													
Art Unit	2165 2185													
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FOREIGN PATENT DOCUMENTS

Examiner Initial	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

NON-PATENT LITERATURE

Examiner Initial	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
A.S.	AH	TANENBAUM, "Structured Computer Organization", 1984, Prentice-Hall, Inc., 2 nd Edition, pp. 10-12.
A.S.	AI	TORRELLAS et al., "False Sharing and Spatial Locality in Multiprocessor Caches", June 1994, IEEE Transactions on Computers, Vol. 43, No. 6, pp. 651-663.
A.S.	AJ	ROTHMAN et al., "Analysis of Shared Memory Misses and Reference Patterns", 2000, IEEE, pp. 187-198.

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<div style="text-align: right; margin-bottom: 10px;"> APR 25 2006 U.S. PATENT AND TRADEMARK OFFICE </div> <div style="text-align: center;"> INFORMATION DISCLOSURE STATEMENT BY APPLICANT </div>	<p>Substitute for form 1449/PTO</p> <p style="text-align: right;">Complete If Known</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 45%;">Application Number</td> <td style="width: 55%;">10/806,871</td> </tr> <tr> <td>Filing Date</td> <td>03-22-2004</td> </tr> <tr> <td>First Named Inventor</td> <td>Dimpsey et al.</td> </tr> <tr> <td>Examiner Name</td> <td>Popovici, Dev <i>Arpan Savla</i></td> </tr> <tr> <td>Art Unit</td> <td>2165 2185</td> </tr> <tr> <td>Attorney Docket No.</td> <td>AUS920040064US1</td> </tr> </table>	Application Number	10/806,871	Filing Date	03-22-2004	First Named Inventor	Dimpsey et al.	Examiner Name	Popovici, Dev <i>Arpan Savla</i>	Art Unit	2165 2185	Attorney Docket No.	AUS920040064US1
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A.S.	AG	Wikipedia "JavaServer Pages" downloaded 1/24/06 http://en.wikipedia.org/wiki/JavaServer_Pages
A.S.	AH	"Hardware Cycle Based memory Residency", IBM, May 22, 2003, ip.com, IPCOM000012728D, pp. 1-2
A.S.	AI	HYDE, "The Art of Assembly Language", 2001, Linux Edition, pp. 247-248, retrieved Mar. 1, 2005 from http://webster.cs.ucr.edu/AoA/Linux/PDFs/0_PDFIndexLinux.html

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Application Number	10/806,871
Filing Date	03-22-2004
First Named Inventor	Dimpsey et al.
Examiner Name	Popovici, Dov
Art Unit	2165
Attorney Docket No.	AUS920040064US1

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A.S.	AA 5394529	02-28-1995	Brown, III et al.	
	AB 6233679 B1	05-15-2001	Holmberg	
	AC 5887159	03-23-1999	Burrows	
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	AM 2004/0153612 A1	08-05-2004	Mutz et al.	
↓	AN 2005/0091456 A1	04-28-2005	Huck	
A.S.	AO 2005/0108483 A1	05-19-2005	Bungo	

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A.S. AP	JEONG et al., "Cost Sensitive Cache Replacement Algorithms", June 2002, Second Workshop on Cashing, Coherence and Consistency, NY, pp. 1-14.

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	First Named Inventor		Dimpsey et al.	
	Art Unit		2165- 2185	
	Examiner Name		Gamm, Jeffrey A. Arpan Savla	
	Attorney Docket Number		AUS920040064US1	

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A.S.	1	6973417	B1	2005-12-06	Maxwell et al.	
A.S.	2	6721875	B1	2004-04-13	McCormick et al.	

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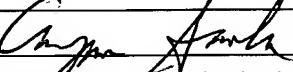
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	Examiner Name	Gaffin, Jeffrey A. Arpen Savela
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